

FIGURE 1A
(PRIOR ART)

100 →

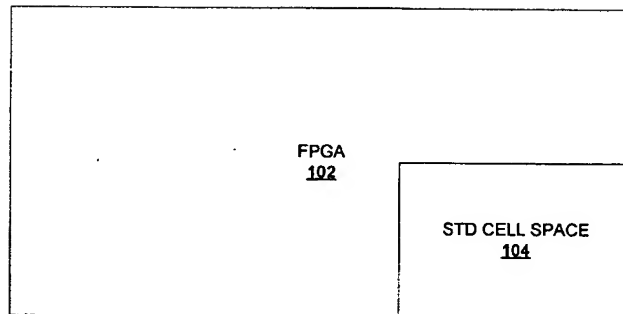


FIGURE 1B

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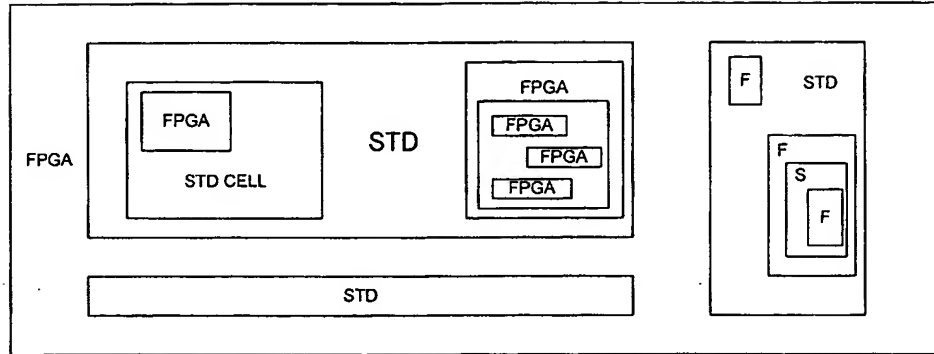


FIGURE 1C

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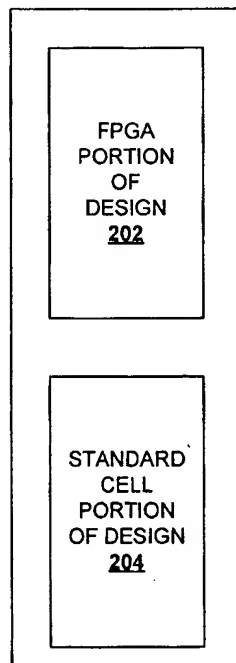
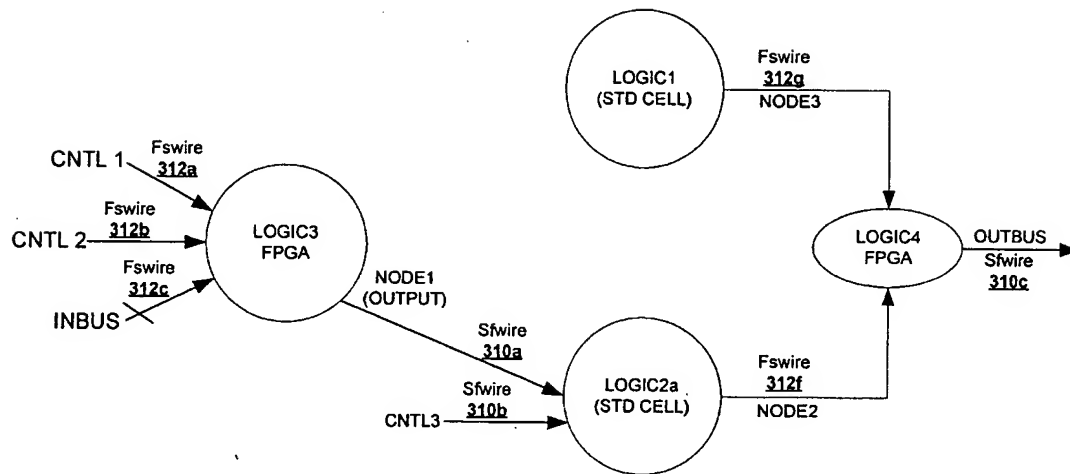


FIGURE 2

WIRE TYPE	MEANING	FIXED OR ADJUSTABLE
(S)wire	STANDARD CEL	FIXED
Fwire	FPGA	FIXED
sFwire	TOOL REPARTITION REQUEST: FPGA -> STD CELL	ADJUSTABLE
fSwire	TOOL REPARTITION REQUEST: STD CELL -> FPGA	ADJUSTABLE
Sfwire	STANDARD CELL, ACCEPTED BY DESIGNER	ADJUSTABLE
Fswire	FPGA, ACCEPTED BY DESIGNER	ADJUSTABLE

FIGURE 3

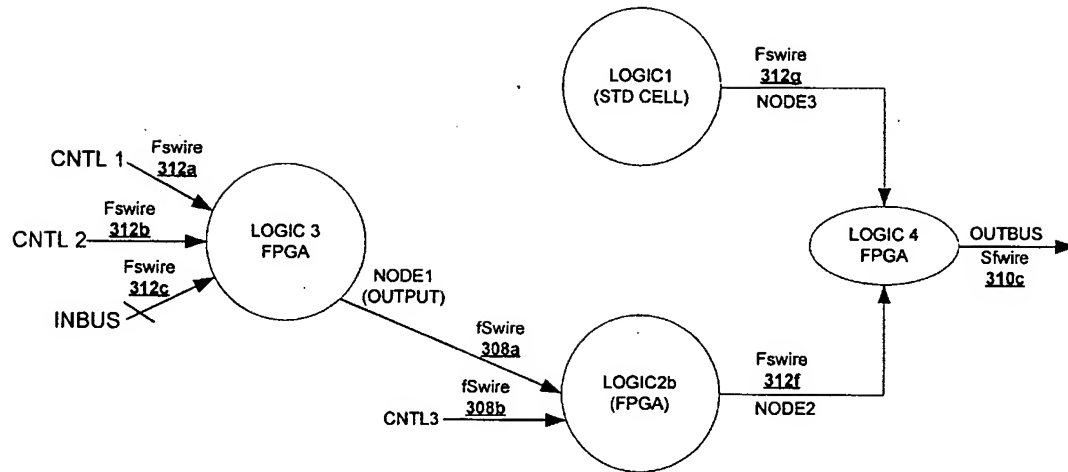
**EXAMPLE VERILOG**

```

module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input Sfwire CNTL3;
Sfwire NODE1;
Fswire NODE2, NODE3;
output Sfwire [7:0] OUTBUS;

```

FIGURE 4A

**EXAMPLE VERILOG**

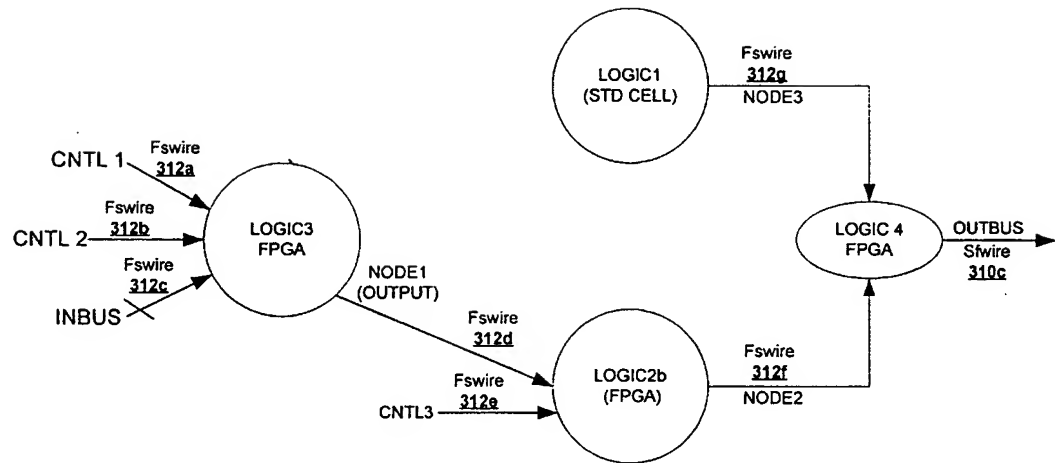
```

module MyDesign (CNTL1, CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input fSwire CNTL3;
fSwire NODE1;
Fswire NODE2, NODE3;
output Sfwire [7:0] OUTBUS;

```

FIGURE 4B

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EXAMPLE VERILOG

```

module MyDesign (CNTL1,CNTL2, INBUS, CNTL3,
OUTBUS);
input Fswire CNTL1, CNTL2;
input Fswire [7:0] INBUS;
input Fswire CNTL3;
Fswire NODE1;
Fswire NODE2, NODE3;
output Sfwire [7:0] OUTBUS;

```

FIGURE 4C

OPTIONS FOR PARTITIONING A STANDARD CELL WIRE

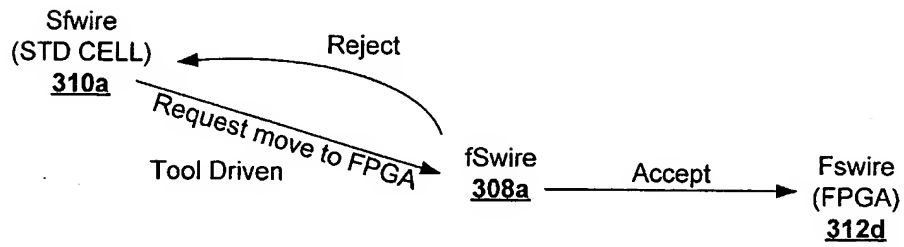


FIGURE 5A

OPTIONS FOR PARTITIONING A STANDARD CELL WIRE

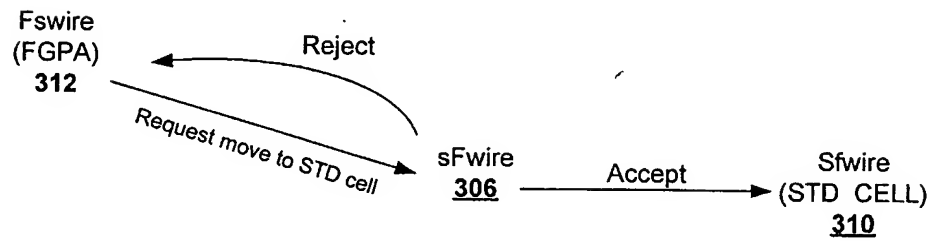


FIGURE 5B

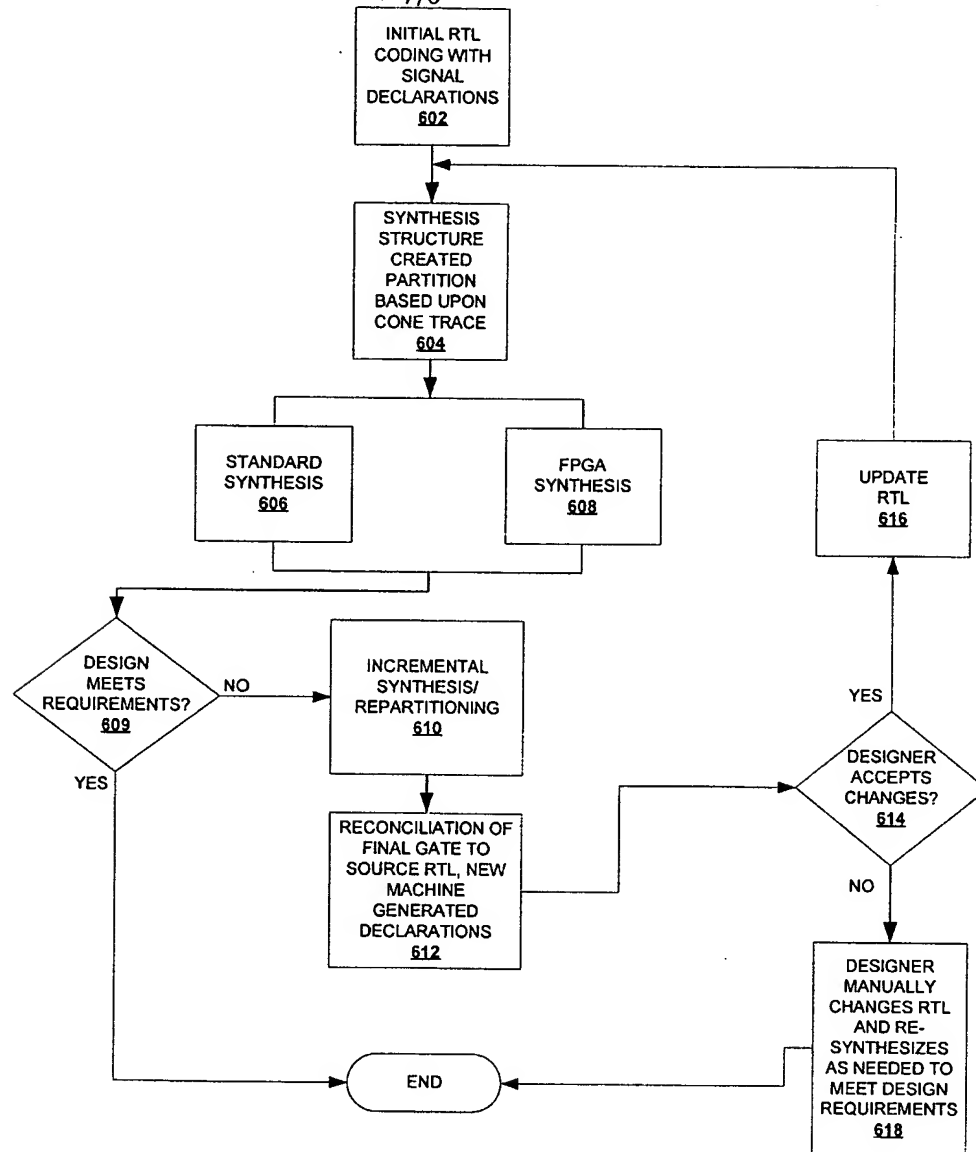


FIGURE 6

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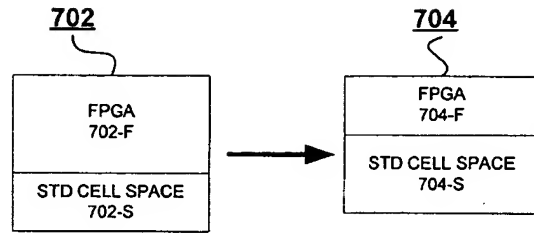


FIGURE 7A

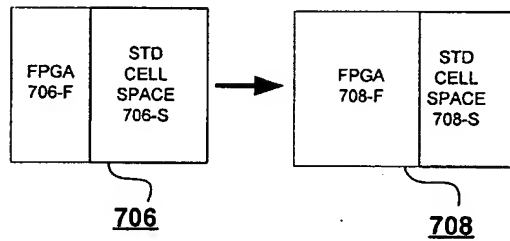


FIGURE 7B